	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	35	((((address$2 with table$2) and ((address$2 with table$2) same (((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4)))) and (second near10 table) and (first near10 table) and (corresponden$4 near10 address$4)) and (third near5 table)) and (new and old)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:57			0
2	BRS	L2	19370	spread$6 near5 time	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:57			0
3	BRS	L3	2576	download$6 near5 table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:58			0
4	BRS	L4	81	l3 and l2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:58			0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
5	BRS	L5	0	l1 and l4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:58			0
6	BRS	L6	268	((address$2 with table$2) and ((address$2 with table$2) same (((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4)))) and (second near10 table) and (first near10 table) and (corresponden$4 near10 address$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:59			0
7	BRS	L7	0	l4 and l6	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/26 10:59			0

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
1	US 20040187117 A1	20040923	99	Handling interrupts in data processing	718/100	710/260	Orion, Luc et al.
2	US 20040181682 A1	20040916	96	Diagnostic data capture control for multi-domain processors	713/200		Orino, Luc et al.
3	US 20040177269 A1	20040909	101	Apparatus and method for managing access to a memory	713/200		Belnet, Lionel et al.
4	US 20040177261 A1	20040909	104	Control of access to a memory by a device	713/193		Watt, Simon Charles et al.
5	US 20040170046 A1	20040902	99	Technique for accessing memory in a data processing apparatus	365/145		Belnet, Lionel et al.
6	US 20040163013 A1	20040819	97	Function control for a processor	714/30		Watt, Simon Charles et al.
7	US 20040158736 A1	20040812	106	Exception types within a secure processing system	713/200		Watt, Simon Charles et al.
8	US 20040158727 A1	20040812	97	Security mode switching via an exception vector	713/193		Watt, Simon Charles et al.
9	US 20040153807 A1	20040805	97	Delivering data processing requests to a suspended operating system	714/35	712/244	Watt, Simon Charles et al.
10	US 20040153672 A1	20040805	100	Switching between secure and non-secure processing modes	713/201		Watt, Simon Charles et al.
11	US 20040153593 A1	20040805	97	Handling multiple interrupts in a data processing system utilising multiple operating systems	710/200		Watt, Simon Charles et al.
12	US 20040148480 A1	20040729	97	Virtual to physical memory address mapping within a system having a secure domain and a non-secure domain	711/163	711/206	Watt, Simon Charles et al.
13	US 20040143720 A1	20040722	102	Apparatus and method for controlling access to a memory	711/206	711/163; 711/207	Mansell, David Hennah et al.
14	US 20040143714 A1	20040722	98	Apparatus and method for controlling access to a memory unit	711/163	711/145	Watt, Simon Charles
15	US 20040139346 A1	20040715	97	Exception handling control in a secure processing system	713/200		Watt, Simon Charles et al.
16	US 20040105298 A1	20040603	107	Apparatus and method for managing processor configuration data	365/149		Symes, Dominic Hugo

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
17	US 20030179712 A1	20030925	1116	CONNECTIONLESS COMMUNICATIONS SYSTEM, ITS TEST METHOD, AND INTRA-STATION CONTROL SYSTEM	370/249	370/250; 370/368; 710/24	KOBAYASHI, YASUSI et al.
18	US 20020193116 A1	20021219	31	Network-layer and link-layer use of shadow addresses with IP-based base stations	455/445		Agrawal, Prathima et al.
19	US 20020193114 A1	20021219	32	Network-layer and link-layer use of shadow addresses in soft handoff within subnets	455/442	370/335	Agrawal, Prathima et al.
20	US 20020191561 A1	20021219	32	Packet distribution and selection in soft handoff for IP-based base stations among multiple subnets	370/331	370/338; 370/349; 370/352; 370/401; 455/442	Chen, Jyh-Cheng et al.
21	US 20020191560 A1	20021219	31	Distributed smooth handoff using shadow addresses in IP-based base stations	370/331	370/338; 370/349; 370/352; 370/401; 455/436	Chen, Jyh-Cheng et al.
22	US 20020191558 A1	20021219	32	Distributed soft handoff among IP-based base stations	370/329	370/473	Agrawal, Prathima et al.
23	US 20020051394 A1	20020502	139	Flash memory control method and apparatus processing system therewith	365/221		Tobita, Tsunehiro et al.
24	US 6715057 B1	20040330	17	Efficient translation lookaside buffer miss processing in computer systems with a large range of page sizes	711/207		Kessler, Richard E. et al.
25	US 6421279 B1	20020716	137	Flash memory control method and apparatus processing system therewith	365/189.01	365/189.04; 365/189.05; 365/233	Tobita, Tsunehiro et al.
26	US 6275436 B1	20010814	136	Flash memory control method and apparatus processing system therewith	365/221	365/189.01; 365/189.05; 365/233; 365/49	Tobita, Tsunehiro et al.
27	US 6078520 A	20000620	136	Flash memory control method and information processing system therewith	365/185.09	365/185.11; 365/185.29; 365/185.33; 365/200; 365/230.03	Tobita, Tsunehiro et al.

	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Inventor
28	US 6049825 A	20000411	17	Method and system for switching between duplicated network interface adapters for host computer communications	709/221	709/220; 714/2	Yamamoto, Shinji
29	US 5973964 A	19991026	136	Flash memory control method and information processing system therewith	365/185.29	365/185.11; 365/189.01; 365/218	Tobita, Tsunehiro et al.
30	US 5963672 A	19991005	79	Data encoding and decoding systems	382/238	348/394.1; 358/539; 382/245; 382/247	Yajima, Akihiko et al.
31	US 5940597 A	19990817	23	Method and apparatus for periodically updating entries in a content addressable memory	709/242	711/149	Chung, David H.
32	US 5862083 A	19990119	136	Information processing system	365/185.09	365/185.11; 365/185.22; 365/189.07; 365/230.03	Tobita, Tsunehiro et al.
33	US 5764804 A	19980609	83	Data encoding and decoding system	382/238	348/27; 348/38; 348/642; 358/426.02; 358/500; 358/539; 359/563; 380/54; 382/131; 382/245; 382/247; 409/165	Yajima, Akihiko et al.
34	US 5530673 A	19960625	136	Flash memory control method and information processing system therewith	365/185.09	365/185.04; 365/185.11; 365/185.22; 365/185.33; 365/201; 714/710; 714/718	Tobita, Tsunehiro et al.
35	US 5428758 A	19950627	14	Method and system for remapping memory from one physical configuration to another physical configuration	711/165	711/202	Salsburg, Linda B.

	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
1	BRS	583824	(add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:23		
2	BRS	596844	(add$4 or modif$4 or remov$4 or updat$4 or replac$6) near5 (equipment or controller or system)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:24		
3	BRS	65279	address$2 with table$2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:26		
4	BRS	583824	((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same ((add$4 or modif$4 or remov$4 or updat$4 or replac$6) near5 (equipment or controller or system))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:26		
5	BRS	1804335	table or matrix or tabulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:27		
6	BRS	33173	((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:27		
7	BRS	7952	(address$2 with table$2) same (((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:27		
8	BRS	7952	(address$2 with table$2) and ((address$2 with table$2) same (((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:28		
9	BRS	84990	second near10 table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:28		
10	BRS	113007	first near10 table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:29		
11	BRS	8849	corresponden$4 near10 address$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:29		
12	BRS	17253	third near5 table	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:30		

	Errors
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	Type	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition
13	BRS	72	(((address$2 with table$2) and ((address$2 with table$2) same (((add$4 or modif$4 or remov$4 or updat$4 or replac$4) near5 (equipment or controller or system)) same (table or matrix or tabulat$4)))) and (second near10 table) and (first near10 table) and (corresponden$4 near10 address$4)) and (third near5 table)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:30		
14	BRS	152083	new and old	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/25 12:30		

	Errors
13	0
14	0